REMARKS

Claims 1-19 and 21-63 are pending in the application. Claims 1-19 and 21-63 are rejected. Claims 1, 55, 58, and 60-63 are amended herein, and no new material is added by the amendments herein. Applicants respectfully submit that claims 1-19 and 21-63, as amended herein, are patentably distinct from the cited prior art and the prior art made of record, and therefore the rejections have been overcome. Thus, Applicants respectfully request withdrawal of the rejections.

Power of Attorney and Correspondence Address

Applicants would like to call to the Examiner's attention that the Office Action mailed December 29, 2003 was not mailed to the Attorneys of record. Applicants include herewith a copy of the Power of Attorney document executed on July 18, 2002, mailed to the United States Patent and Trademark Office (USPTO) on July 24, 2002, and received by the USPTO on August 2, 2002 in which all prior powers were revoked and the practitioners at Shemwell Gregory & Courtney LLP, Customer Number 30554, were appointed as the attorneys of record. **In accordance with the Power of Attorney received by the USPTO on August 2, 2002, Applicants respectfully request that all further communications in this matter be directed to Rick Gregory, Shemwell Gregory & Courtney LLP, 4880 Stevens Creek Boulevard, Suite 201, San Jose, California 95129, telephone (408) 236-6646, facsimile (408) 236-6641.**

Claim Rejections Under 35 USC §132

The Examiner objects to Applicant's amendment filed June 4, 2004 under 35 U.S.C. §132 because it introduces new matter into the disclosure. Applicants however respectfully submit that the language of "an operating system layer including non-real-time processes" is supported by the original disclosure and is therefore not new matter. Applicants direct the Examiner to Figures 11, 15, and 16 of the original disclosure along with the portions of the disclosure corresponding to these figures. As one example, page 21, lines 4-15 reads as follows:

> "The preprocessor 1104 of an embodiment is a hardware device

that facilitates the separation between lower level programming and higher level programming, while also permitting lower power operation. The preprocessor 1104 is coupled between at least one high level processor 1102 and devices or functions of the network that are linked to the physical world and require real-time operation. The devices or functions of the network that are linked to the physical world include, but are not limited to, the sensor suite 1106, the communication devices 1108, the signal processors and storage devices 1110, the power or energy supplies 1112, and the actuation suite 1114. Each node may include a number of combinations and variations of the sensor suite 1106, the communications devices 1108, the signal processors and storage devices 1110, the power supplies 1112, and the actuation suite 1114."

This example passage recites "real-time" operation, and thus Applicants respectfully submit that their reference to processes or operations exclusive of real-time operations as "non-real-time" is supported by the original disclosure and is therefore not new matter. However, in the interest of clarity, Applicants herein amend the claims to amend reference to "non-real-time" to "remaining processes other than the real-time processes".

Claim Rejections Under 35 USC §112

Claims 1, 55, 58, 60, and 61-63 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Applicants herein amend claims 1, 55, 58, 60, and 61-63 to overcome this rejection, as described above with reference to the objection under 35 U.S.C. §132. Applicants therefore request removal of this rejection.

Claim Rejections Under 35 USC §103

Claims 1, 3, 9, 12-17, 19, 21-24, 26-28, 33-35, 37-40, 42-45, 47, 50, 52, 53, and 55-63 are rejected under 35 USC §103(a) as being unpatentable over Clare et al., United States Patent number 6,414,955 ("Clare"), in view of Creekmore et al., United States Patent number 5,534,697 ("Creekmore"), and Azarya et al., United States Patent number

5,978,578 ("Azarya"). The Examiner asserts that Clare taught collecting and processing data in a sensor network, comprising: coupling a plurality of network elements including at least one node among an environment and at least one client computer; collecting data from the environment; remotely controlling at least one function of the at least one node; providing node information including node resource costs and message priority from the at least one node to the plurality of network elements; and distributing processing of the collected data among the plurality of network elements in response to the node information.

The Examiner states however that Clare does not teach a preprocessor operating on real-time processes. However, the Examiner opines that, because Creekmore taught a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor, it would have been obvious to combine the teaching of Clare and Creekmore because Creekmore's system of a preprocessor operating on real-time processes would increase efficiency of Clare's system by providing temporal filtration of real-time data to minimize the data link transmission rates.

The Examiner further states that Clare and Creekmore did not teach application program interfaces (APIs). However, the Examiner opines that, because Azarya taught configuring the node at one of a plurality of programming layers through a plurality of APIs, it would have been obvious to combine the teaching of Clare, Creekmore, and Azarya because Azarya's system of using APIs would increase the flexibility of the Clare and Creekmore systems by allowing a user to customize a routine to access data through the application connectivity layer.

The Examiner further states that the combination of Clare, Creekmore, and Azarya did not teach programming layers including a physical layer that includes real-time processes and an operating system layer that includes non-real-time processes. The Examiner asserts that Azarya taught a system for providing computer operated real-time process control with the means for interacting with an external system. The Examiner also takes Official Notice of the concept of a physical layer performing real-time processes with an external network and a layer performing non-real-time processes as being known and accepted in the art. The Examiner therefore opines that it would have

been obvious to use a physical layer to communicate with an external network and a layer for performing non-real-time processes because this would increase the adaptability of the system with the International Organization for Standardization Open System Interconnection (ISO/OSI) model.

Applicants respectfully submit that Clare discloses a wireless network of communicating devices including nodes, and agree with the Examiner that Clare fails to teach or suggest a preprocessor operating on real-time processes. Creekmore describes an electro-optical sensor system for use in observing objects. The sensor system of Creekmore includes a pre-processor system connected to a staring sensor. A data link transmits data from the pre-processor to a data interpretation and discrimination module. The pre-processor provides temporal filtration of real-time observations in order to minimize the data link transmission rates. The data interpretation and discrimination module presents the data to the operator for his understanding and control of the sensor as well as dissemination of information to field operators. The data interpretation and discrimination module feeds back commands to control the remote system controller. The remote system controller translates the desired modifications of aggregation into the pre-processor system format. Creekmore, column 3, lines 1-20.

Applicants submit that Creekmore describes each of the remote system controller and data interpretation and discrimination module as being separate and apart from the pre-processor. Therefore, any processor included in the remote system controller and/or data interpretation and discrimination module does not include the pre-processor. Applicants fail to find any reference in Creekmore to an embodiment in which the pre-processor includes a processor of the remote system controller and/or data interpretation and discrimination module. Additionally, Applicants fail to find any reference in Creekmore to an embodiment in which the remote system controller and/or data interpretation and discrimination module include the pre-processor. Consequently, Creekmore fails to disclose a single component that includes both the pre-processor and any processor included in the remote system controller and/or data interpretation and discrimination module.

As further support, Creekmore describes an embodiment in which the sensor, cooler, and pre-processor are fixedly attached to a remote post or sensor mount while the

remote system controller and data interpretation and discrimination module are located at a dispatch center (Creekmore, column 4, lines 3-14; figure 5). Additionally, Creekmore describes another embodiment in which the sensor, cooler, and pre-processor are located on an external portion of an aircraft while the remote system controller and data interpretation and discrimination module reside within the aircraft (Creekmore, column 4, lines 40-57; figure 6). Thus, Creekmore fails to teach or suggest a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor (emphasis added).

Regarding a combination of teachings in Clare and Creekmore, Applicants fail to identify any suggestion or motivation to combine these two references. Clare describes a wireless network of communicating devices that uses a distributed method of topology learning to organize multiple-hop, relayed communication among the devices. The methods taught by Clare identify interference neighbors and communication neighbors for each device of a network of devices, preferably using ranging between devices and distributed calculation to limit the number of devices involved in each step of the topology learning method, thereby conserving energy and bandwidth (Clare, column 6, lines 6-31; Abstract).

In contrast to Clare, Creekmore describes a sensor system for use in observing objects. Applicants fail to find any reference in Creekmore to a network of devices or to network communications involving the sensor system of Creekmore. Therefore, because Clare describes systems and methods for communicating among a network of devices, and Creekmore describes a single sensor system with no mention of use of this system in or with a network, there would be no motivation or suggestion to combine the references.

Even assuming a motivation to combine Clare and Creekmore, as the Examiner suggests, the combination would fail to teach or suggest a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor (emphasis added). Combination of the teachings of Creekmore with those of Clare would instead provide a first node of the Clare system having only a pre-processor (or processor) and a second node of the Clare system having only a processor (or pre-processor). Thus, the combination of Clare and Creekmore would not teach or suggest a node comprising at least one preprocessor operating on real-time processes and

at least one processor coupled to the preprocessor. Applicants therefore respectfully submit that the invention claimed in claim 1 would not have been obvious to one of ordinary skill in view of Clare and Creekmore, alone and/or in any combination.

In addition to Applicants assertion that Clare and Creekmore do not describe a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor, the Examiner states that Clare and Creekmore do not teach APIs. In addressing the Examiner's assertion that Azarya taught configuring the node at one of a plurality of programming layers through a plurality of APIs, Applicants respectfully submit that Azarya does not teach configuring a node at one of a plurality of programming layers through a plurality of APIs.

Applicants submit that Azarya describes a control automation system for enabling I/O boards to access communication networks for receiving and transmitting real-time control information over a communication network. As for teachings of Azarya relating to APIs, Applicants only find two references in Azarya to their use of APIs. In a first reference to APIs, Azarya discloses that, using open APIs, devices within an intranet share process data and device status information with other nodes via the intranet or the internet (Azarya, column 6, lines 60-62). In a second reference to APIs, Azarya discloses that a set of high level APIs can be written that allow each processor, controller or computer connected to the area network of the Internet to access sensor information at the application connectivity layer (Azarya, column 9, lines 22-25). As neither of the references to APIs found in Azarya describe configuring a node at one of a plurality of programming layers through a plurality of APIs, Applicants submit that Azarya fails to teach or suggest a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor, and configuring the node at one of a plurality of programming layers through a plurality of APIs (emphasis added).

Regarding a combination of teachings in Clare, Creekmore, and Azarya, Applicants fail to see any suggestion or motivation to combine these three references, as described above. Even assuming a motivation to combine Clare, Creekmore, and Azarya as the Examiner suggests, the combination would fail to teach or suggest a node comprising at least one preprocessor operating on real-time processes and at least one

processor coupled to the preprocessor, and configuring the node at one of a plurality of programming layers through a plurality of APIs (emphasis added). Combination of the teachings of Creekmore with those of Clare would instead provide a first node of the Clare system having only a pre-processor (or processor) and a second node of the Clare system having only a processor (or pre-processor). Further combining the teachings of Azarya, one or more of the first and second nodes may include APIs that allow each processor, controller or computer connected to a network that includes the nodes to access sensor information of one or more of the first and second nodes. Thus, the combination of Clare, Creekmore, and Azarya would not teach or suggest a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor, and configuring the node at one of a plurality of programming layers through a plurality of APIs. Applicants therefore respectfully submit that the invention claimed in claim 1 would not have been obvious to one of ordinary skill in view of Clare, Creekmore, and Azarya alone and/or in any combination.

The Examiner states that the combination of Clare, Creekmore, and Azarya also do not teach programming layers including a physical layer that includes real-time processes and an operating system layer that includes non-real-time processes. The Examiner asserts that Azarya taught a system for providing computer operated real-time process control with the means for interacting with an external system. The Examiner also takes Official Notice of the concept of a physical layer performing real-time processes with an external network and a layer performing non-real-time processes as being known and accepted in the art.

Applicants submit that while there are many ways to partition hardware and software functionality, it is not obvious or "officially noticed" how to do so for a particular architecture and/or set of applications. Azarya describes an OpenBus automation system in which control algorithms and logic flow that a user desires to implement are executed by a real-time kernel in a target system (Azarya, column 18, line 58 to column 19, line 8). Surrounding the real-time kernel of the target system is an operating system (OS), and a layer surrounding the OS includes various functional modules that perform various roles in the OpenBus system (Azarya, column 19, lines 15-20). Applicants submit that Azarya however teaches away from the invention of claim 1

because Azarya fails to disclose a target system comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor, and configuring the node at one of a plurality of programming layers through a plurality of APIs, wherein the programming layers include a physical layer including real-time processes and an operating system layer that operates on remaining processes other than the real-time processes.

As described above, Applicants fail to see any suggestion or motivation to combine Clare, Creekmore, and Azarya. Even assuming a motivation to combine Clare, Creekmore, and Azarya as the Examiner suggests, the combination would fail to teach or suggest a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor, and configuring the node at one of a plurality of programming layers through a plurality of APIs (emphasis added). Combination of the teachings of Creekmore with those of Clare would instead provide a first node of the Clare system having only a pre-processor (or processor) and a second node of the Clare system having only a processor (or pre-processor). Further combining the teachings of Azarya, one or more of the first and second nodes may include APIs that allow each processor, controller or computer connected to a network that includes the nodes to access sensor information of one or more of the first and second nodes. Thus, the combination of Clare, Creekmore, and Azarya would not teach or suggest a node comprising at least one preprocessor operating on real-time processes and at least one processor coupled to the preprocessor, and configuring the node at one of a plurality of programming layers through a plurality of APIs, wherein the programming layers include a physical layer including real-time processes and an operating system layer that operates on remaining processes other than the real-time processes. Applicants therefore respectfully submit that the invention claimed in claim 1 would not have been obvious to one of ordinary skill in view of Clare, Creekmore, and Azarya alone and/or in any combination.

Additionally, as claims 2-19 and 21-54 depend from claim 1, claims 2-19 and 21-54 are patentable over Clare, Creekmore, and Azarya alone and/or in any combination. Furthermore, as claim 55 includes limitations similar to those of claim 1, and claims 56 and 57 depend from claim 55, claims 55-57 are also patentable over Clare, Creekmore,

and Azarya alone and/or in any combination. Additionally, as claim 58 includes limitations similar to those of claim 1, and claim 59 depends from claim 58, claims 58 and 59 are also patentable over Clare, Creekmore, and Azarya alone and/or in any combination. Moreover, as claims 60-63 each include limitations similar to those of claim 1, claims 60-63 are also patentable over Clare, Creekmore, and Azarya alone and/or in any combination. Accordingly, Applicants respectfully request withdrawal of the rejection under 35 USC §103(a).

Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that claims 1-19 and 21-63 as presented herein are in condition for allowance. Thus, allowance of the claims is requested. If in the opinion of Examiner Lee a telephone conference would expedite the prosecution of the subject application, or if there are any issues that remain to be resolved prior to allowance of the claims, Examiner Lee is encouraged to call Rick Gregory at (408) 236-6646.

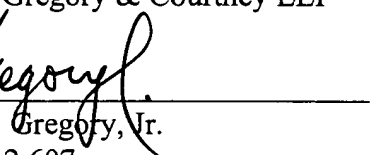
A Petition for Extension of Time Under 37 CFR 1.136(a) is enclosed herewith in duplicate for a three month extension of time.

AUTHORIZATION TO CHARGE DEPOSIT ACCOUNT

Please charge deposit account 501914 for any fees due in connection with this Office Action response.

Respectfully submitted,
Shemwell Gregory & Courtney LLP

Date: March 21, 2005



Richard L. Gregory, Jr.
Reg. No. 42,607
Tel. 408-236-6646